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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/955,874	09/18/2001	Mika Salmi	874.0100.U1(US)	9941

29683 7590 12/26/2002

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EXAMINER
NGUYEN, LINH V

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 12/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/955,874	SALMI ET AL.	
	Examin r	Art Unit	
	Linh V Nguyen	2819	

-- Th MAILING DATE of this communication app ars on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 May 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Objections

1. Claims 14, and 15 objected to because of the following informalities: Claims 14, and 15 are duplicated. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. Claims 5, 9, and 10 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding to claim 5 on page 11, the paragraph " without increasing the current consumption of frequency divider circuits that comprise the phase lock loop" applicant fails to point out the subject matter of how to without increasing the current consumption of frequency divider by using output signal of voltage-controlled-oscillator. Therefore, examiner will disregards this paragraph on this office action.

Regarding to claim 9 on page 11, the paragraph " using the output signal of the oscillator to equalize a delay added in different modes of prescaler 's function" applicant's fails to point out the subject matter of how to equalize a delay added in different modes of prescaler's function by using the output of oscillator. Therefore examiner will disregards this paragraph on this office action.

Regarding to claim 10, on page 12, the method of equalized the delay without increasing the current consumption frequency divider circuits that comprises the phase lock loop. Applicant fails to point out the subject matter of how to equalize the delay

without increasing the current consumption of frequency divider. Therefore this claimed is rejected under rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 3, 5, 6, 7, 9, 11 and 12, are rejected under 35 U.S.C. 102(b) as being anticipated by Cok et al., U.S. patent No. 4,573,023

Regarding to claim 1, Fig. 2 Cok et al disclose a prescaler circuit for use in a frequency source, comprising an input node (From 22) for receiving an input signal having a characteristic frequency to be divided, an output node (60, 58) for outputting a frequency divided signal to an output of the frequency source, and at least one divider stage (52) coupled between the input node and the output node for dividing the input signal by a predetermined amount, and further comprising at least one resampling stage (55 prescaler synchronizer) for receiving an output signal (60) from said at least one divider stage (52), and for synchronizing edges of the output signal to edges of the input signal (Col. 5 lines 19-30) .

Regarding to claim 2, Fig. 1 Cok et al. disclose a phase locked loop comprising a phase comparator (14) generating an output signal that is used to drive a voltage controlled oscillator (18), and a modulus N prescaler (34) circuit coupled to an output of said voltage controlled oscillator (20), said prescaler circuit comprising an input node (From 22) for coupling to said voltage controlled oscillator for receiving an input signal having a characteristic frequency to be divided by N_2, an output node (output form 44) for outputting a frequency divided signal that is coupled to said phase comparator (14), and a plurality of divider stages (50, 52) coupled between the input node and the output node for dividing the input signal by **N**, and further comprising at least one resampling stage (55) coupled to an output of at least one of said divider stages (52) for receiving an output signal therefrom and for synchronizing edges of the output signal to edges of the input signal (Col. 5 lines 19-30), thereby reducing temporal ambiguity in the occurrence of the edges of the output signal.

Regarding to claim 3, wherein the value of **N** is programmable (Col. 4 lines 49 – 55).

Regarding to claim 5, Cok et al. disclose a method of frequency source of a mobile station, comprising: operating a phase locked loop (Fig. 1) as part of the frequency source to generate a signal having a desired frequency (20), the step of operating the phase locked loop including a step of dividing a frequency of an output signal of a voltage controlled oscillator (20) by a predetermined amount (N1, N0); and resampling (55) the frequency divided signal using the output signal of the voltage controlled oscillator to reduce jitter in the frequency divided signal .

Regarding to claim 6, wherein the step of resampling operates a modulus N prescaler circuit (34) that is coupled to the output of the voltage controlled oscillator, the prescaler circuit comprising an input node (From 22) for coupling to the output of the voltage controlled oscillator for receiving an input signal having a characteristic frequency to be divided by N (12), an output node for outputting a frequency divided signal (from 44) that is coupled to a phase comparator (14) of the phase locked loop, and a plurality of the frequency divider circuits (N1, N0) coupled between the input node and the output node for dividing the input signal by N, where the step of resampling is accomplished in a resampling stage (55) coupled to an output of at least one of the frequency divider circuits (52, 55) for receiving an output signal therefrom ,and for synchronizing edges of the output signal to edges of the input signal (Col. 5 lines 19-30), thereby reducing jitter of the output signal (advantages or improvement only not a subject matter).

Regarding to claim 7, wherein the value of N is programmable (Col. 4 lines 49 – 55).

Regarding to claim 9. Fig. 1 Cok et al. disclose a method for operating a phase locked loop as part of the frequency source to generate a signal having a desired frequency, comprising: operating a multi-modulus prescaler function of the phase locked loop to divide a frequency of an output signal of an oscillator by a predetermined amount (52, 50); and resampling the frequency divided signal (55).

Regarding to claim 11 wherein the step of resampling operates a prescaler circuit (55) that is coupled to the output of the oscillator (18), the prescaler circuit comprising

an input node (From 22) for coupling to the output of the oscillator for receiving an input signal having a characteristic frequency to be divided by N (12), an output node (From 44) for outputting a frequency divided signal that is coupled to a phase comparator (14) of the phase locked loop, and a plurality of the frequency divider circuits (52, 50) coupled between the input node and the output node for dividing the input signal by N, where the step of resampling is accomplished in a resampling stage (55) coupled to an output of at least one of the frequency divider circuits for receiving an output signal therefrom and for synchronizing edges of the output signal to edges of the input signal (Col. 5 lines 19-30), thereby equalizing the delay added in different modes of the multi-modulus prescaler function (advantages/improvement only, not a subject matter).

Regarding to claim 12, wherein the value of N is programmable (Col. 4 lines 49 – 55).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4, 8 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cok et al., as applied to claims 1, 5, and 10 above, and in view of Hunt, Jr. et al. U.S. patent No. 6,385,276

Fig. 2 Cok et al. further disclose in the resampling stage (55) is having D-type Flip-Flop (62). However Cok et al fails to teach that the D Flip-Flop is clocked with said input signal.

Fig. 5 Hunt, Jr. et al. disclose a prescaler comprising a resampling stage (515, 555, 557) wherein the resampling having a D Flip-Flop (557) is clocked with a input signal (Fin (520)).

Cok et al. and Hunt, Jr et al. are analogous, because they are from similar area of prescaler with synchronizing circuit. Therefore it would have been obvious to one having ordinary skill in the art at the invention was made to have the D Flip-Flop from Synchronized circuit of Cok et al. clocked with a input signal, which has taught from the synchronized circuit of Hunt, Jr et al. for the purpose of providing high speed prescaler operating at low power levels and low supply voltage that realize benefits of optimized performance of high-speed dual modules dividers (Hunt, Jr. Col. 3 lines 42 – 45).

7. Claims 14 – 16, are rejected under 35 U.S.C. 103(a) as being unpatentable over Cok et al., as applied to claim 9 above.

Cok et al. disclose a PLL with prescaler function to produce a desired frequency signal as applied to claim 9 above, comprising every aspect of applicant's claimed invention, except for explicitly teach a mobile station using the PLL circuit. However, a mobile station is only the intended of use and well knows for transceiver system is using PLL circuit (Applicant's IDS cited arts (Rapeli US5991605, or Jorgensen US5889443)). Furthermore it has been held that a recitation with respect to the manner in which a

claimed apparatus is intend to be employed does not differentiate the claimed apparatus from prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham, 2 USPQ2d 1647 (1987)*

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (703) 305-1934. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

LVN

December 21, 2002

Michael J. Tokar

Michael Tokar
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